Vendor-independent, scalable rules (MOSIS SCMOS Rules)

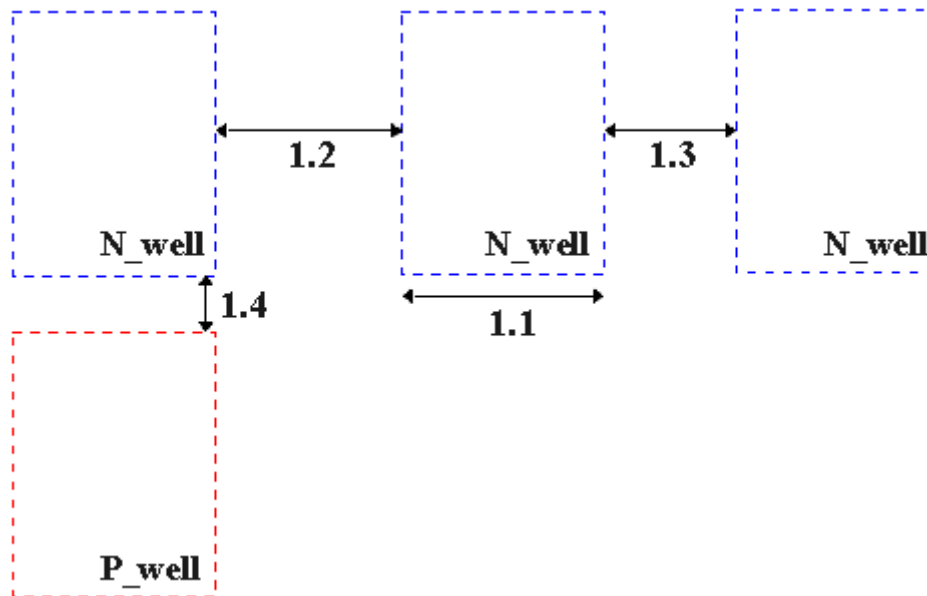**Design Rules**

MOSIS Scalable CMOS (SCMOS)

(Revision 8.00)

Updated: May 11, 2009

This is an abbrevited set of most basic rules for the purpose of early laboratory experiments in EE 330.

SCMOS Layout Rules - Well

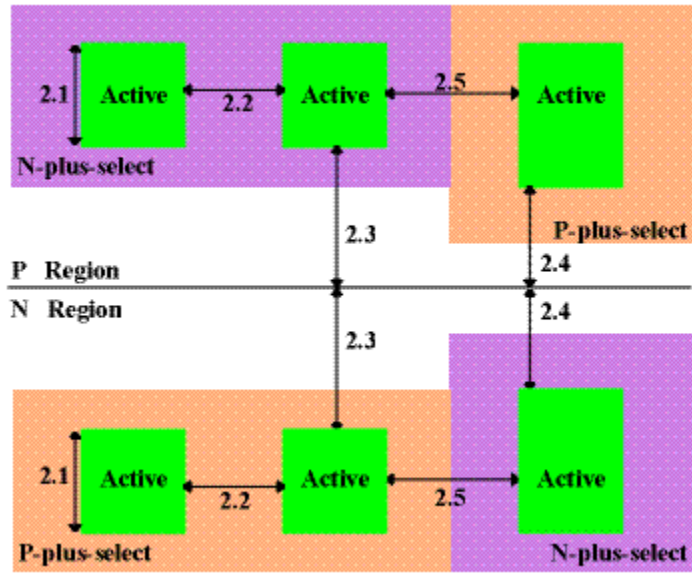| Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
1.1	Minimum width	10	12	12
1.2	Minimum spacing between wells at different potential	9	18	18
1.3	Minimum spacing between wells at same potential	6	6	6
1.4	Minimum spacing between wells of different type (if both are drawn)	0	0	0

SCMOS Layout Rules - Active

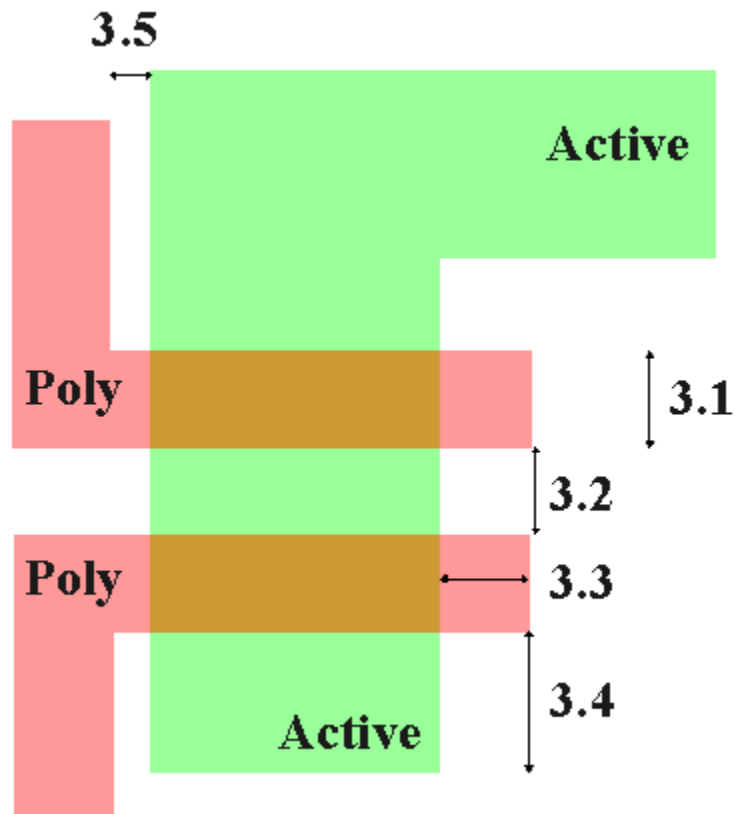| Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
2.1	Minimum width	3 *	3 *	3
2.2	Minimum spacing	3	3	3
2.3	Source/drain active to well edge	5	6	6
2.4	Substrate/well contact active to well edge	3	3	3
2.5	Minimum spacing between non-abutting active of different implant. Abutting active ("split-active") is illustrated under Select Layout Rules.	4	4	4

* Note: For analog and critical digital designs, MOSIS recommends the following minimum MOS channel widths (active under poly) for ON Semiconductor designs. Narrower devices, down to design rule minimum, will be functional, but their electrical characteristics will not scale, and their performance is not predictable from MOSIS SPICE parameters.

Process	Design Technology	Design Lambda (micrometers)	Minimum Width (lambda)
AMI_C5F/N	SCN3M, SCN3ME	0.35	9
AMI_C5F/N	SCN3M_SUBM, SCN3ME_SUBM	0.30	10

SCMOS Layout Rules - Poly

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
3.1	Minimum width	2	2	2
3.2	Minimum spacing over field	2	3	3
3.2.a	Minimum spacing over active	2	3	4
3.3	Minimum gate extension of active	2	2	2.5
3.4	Minimum active extension of poly	3	3	4
3.5	Minimum field poly to active	1	1	1

SCMOS Layout Rules - Select

| Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
4.1	Minimum select spacing to channel of transistor to ensure adequate source/drain width	3	3	3
4.2	Minimum select overlap of active	2	2	2
4.3	Minimum select overlap of contact	1	1	1.5
4.4	Minimum select width and spacing (Note: P-select and N-select may be coincident, but must *not* overlap) (not illustrated)	2	2	4
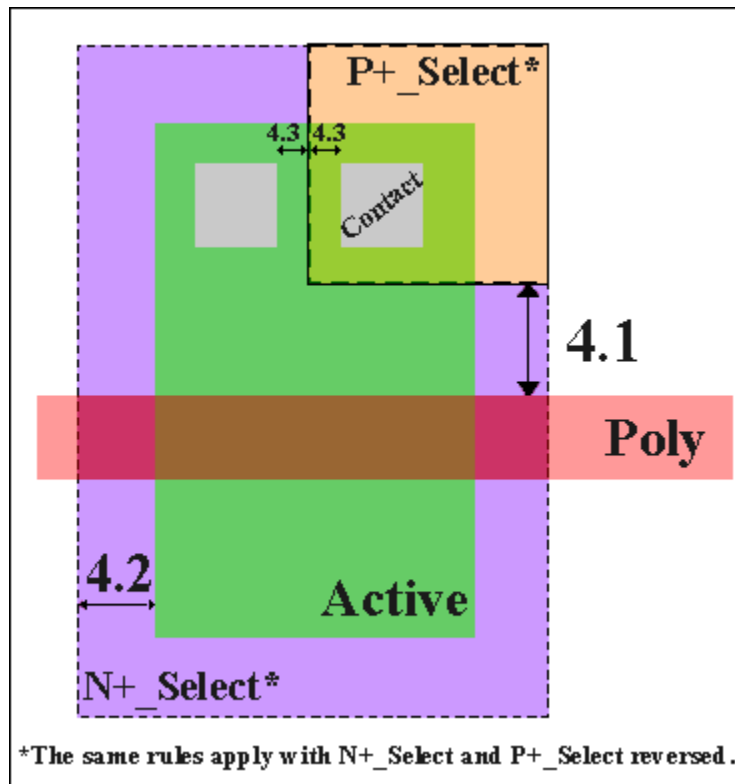
SCMOS Layout Rules - Contact to Poly

On 0.50 micron process (and all finer feature size processes), it is required that all features on the insulator layers (CONTACT, VIA, VIA2) must be of the single standard size; there are no exceptions for pads (or logos, or anything else); large openings must be replaced by an array of standard sized openings. Contacts must be drawn orthogonal to the grid of the layout. Non-Manhattan contacts are not allowed.

If your design cannot tolerate 1.5 lambda contact overlap in 5.2, use the alternative rules which reduce the overlap but increase the spacing to surrounding features. Rules 5.1, 5.3, and 5.4, still apply and are unchanged.
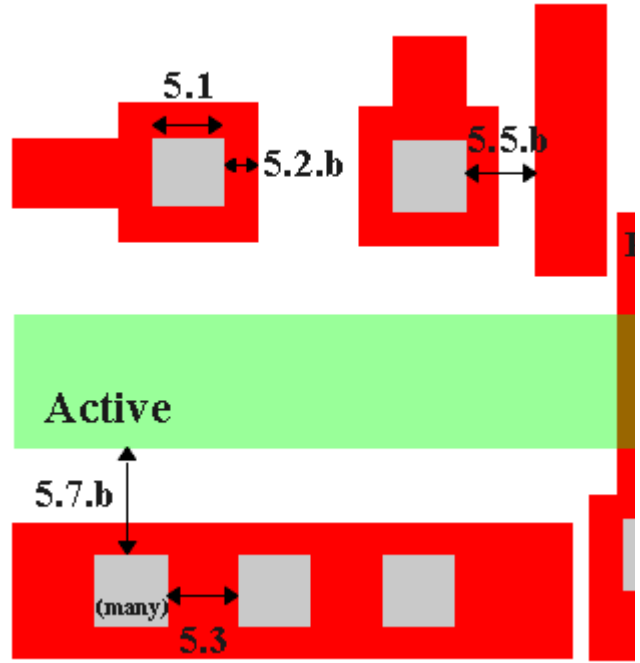
Simple Contact to Poly

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
5.1	Exact contact size	2x2	2x2	2x2
5.2	Minimum poly overlap	1.5	1.5	1.5
5.3	Minimum contact spacing	2	3	4
5.4	Minimum spacing to gate of transistor	2	2	2

Alternative Contact to Poly

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
5.2.b	Minimum poly overlap	1	1	1
5.5.b	Minimum spacing to other poly	4	5	5
5.6.b	Minimum spacing to active (one contact)	2	2	2
5.7.b	Minimum spacing to active (many contacts)	3	3	3

Active

5.4

5.1

Contact

5.1

5.2.b

5.5.b

Active

5.7.b

(many)

5.3
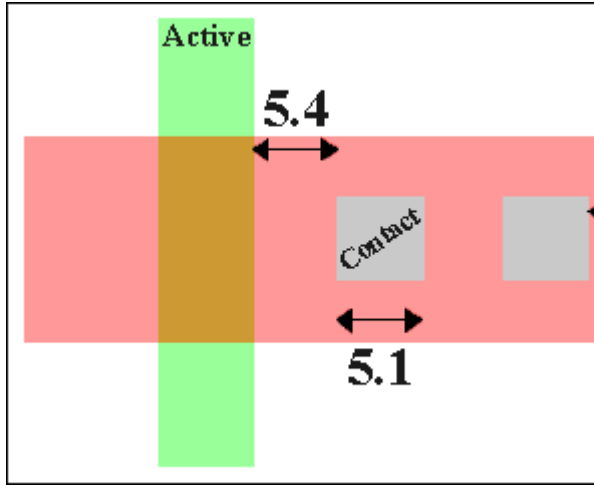
Simple Poly to Contact
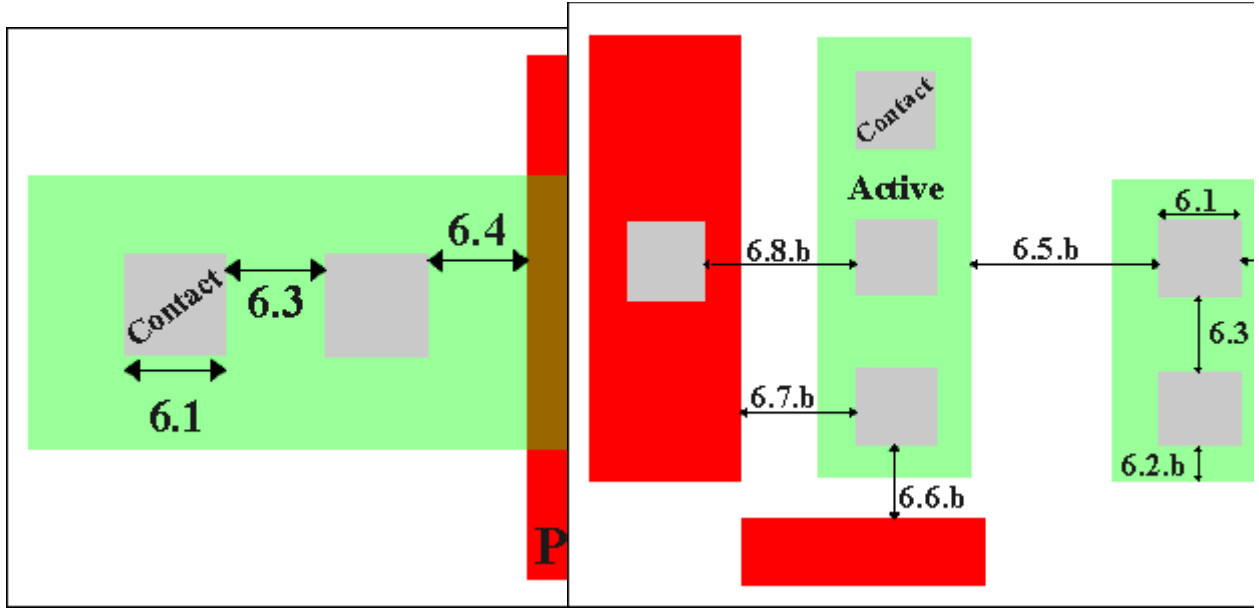
Alternative Contact to Poly

SCMOS Layout Rules - Contact to Active

If your design cannot handle the 1.5 lambda contact overlap in 6.2, use the alternative rules which reduce the overlap but increase the spacing to surrounding features. Rules 6.1, 6.3, and 6.4, still apply and are unchanged. Contacts must be drawn orthogonal to the grid of the layout. Non-Manhattan contacts are not allowed.

Simple
Contact to Active

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
6.1	Exact contact size	2x2	2x2	2x2
6.2	Minimum active overlap	1.5	1.5	1.5
6.3	Minimum contact spacing	2	3	4
6.4	Minimum spacing to gate of transistor	2	2	2

Alternative
Contact to Active

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
6.2.b	Minimum active overlap	1	1	1
6.5.b	Minimum spacing to diffusion active	5	5	5
6.6.b	Minimum spacing to field poly (one contact)	2	2	2
6.7.b	Minimum spacing to field poly (many contacts)	3	3	3
6.8.b	Minimum spacing to poly contact	4	4	4

Simple Contact to Active   Alternative Contact to Active

SCMOS Layout Rules - Metal1

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
7.1	Minimum width	3	3	3
7.2	Minimum spacing	2	3	3
7.3	Minimum overlap of any contact	1	1	1
7.4	Minimum spacing when either metal line is wider than 10 lambda	4	6	6
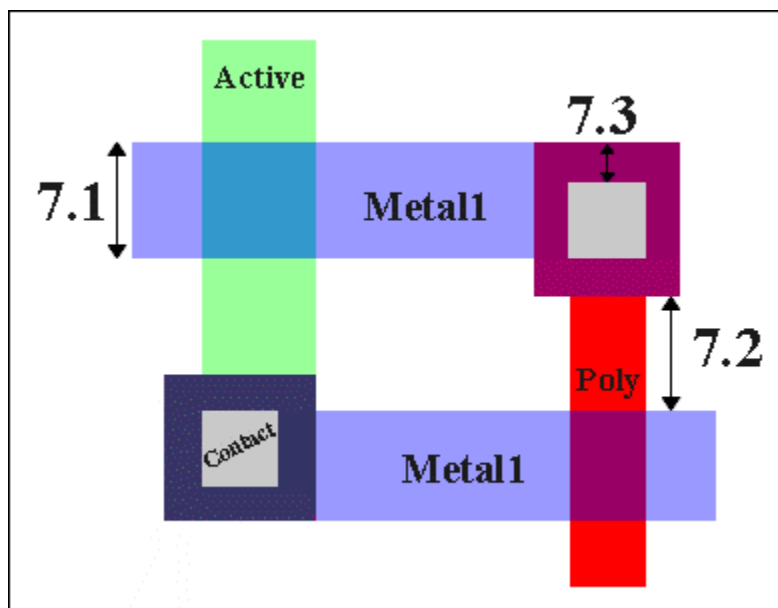
SCMOS Layout Rules - Via
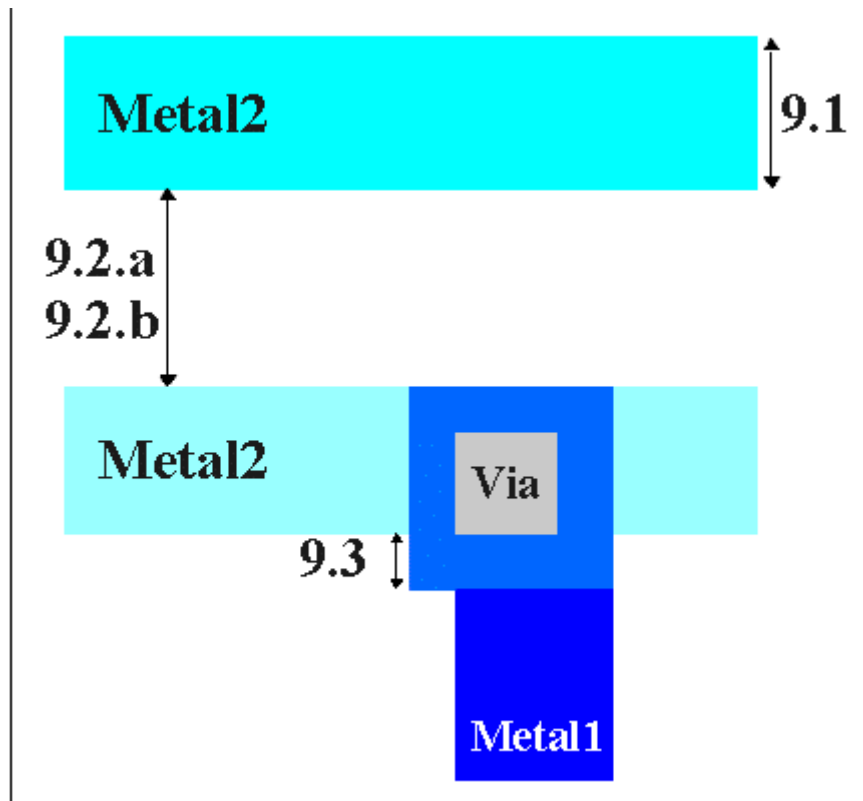
Vias must be drawn orthogonal to the grid of the layout. Non-Manhattan vias are not allowed.

| Rule	Description	Lambda					
		2 Metal Process			3+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
8.1	Exact size	2 x 2	n/a	n/a	2 x 2	2 x 2	3 x 3
8.2	Minimum via1 spacing	3	n/a	n/a	3	3	3
8.3	Minimum overlap by metal1	1	n/a	n/a	1	1	1
8.4	Minimum spacing to contact for technology codes mapped to processes that do not allow stacked vias (SCNA, SCNE, SCN3M, SCN3MLC)	2	n/a	n/a	2	2	n/a
8.5	Minimum spacing to poly or active edge for technology codes mapped to processes that do not allow stacked vias (NOTE: list is not same as for 8.4)	2	n/a	n/a	2	2	n/a
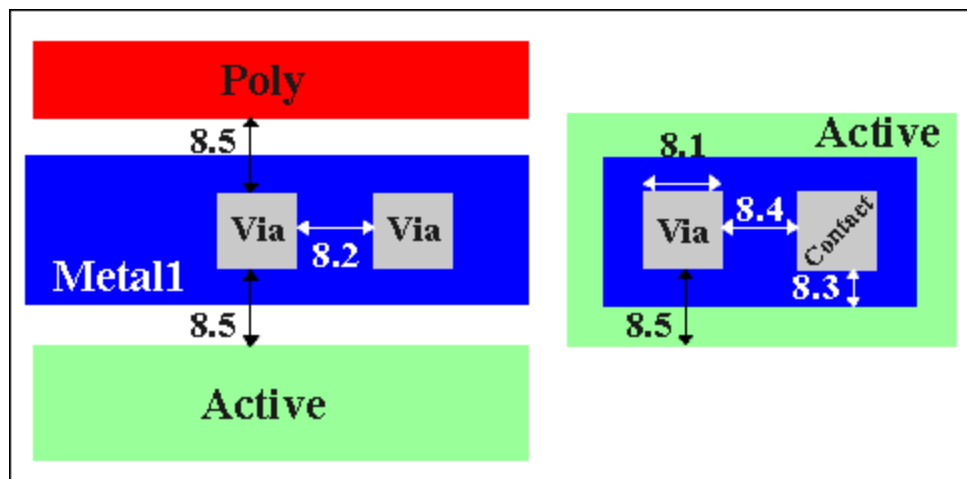
SCMOS Layout Rules - Metal2

Rule	Description	Lambda					
		2 Metal Process			3+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
9.1	Minimum width	3	n/a	n/a	3	3	3
9.2	Minimum spacing	3	n/a	n/a	3	3	4
9.3	Minimum overlap of via1	1	n/a	n/a	1	1	1
9.4	Minimum spacing when either metal line is wider than 10 lambda	6	n/a	n/a	6	6	8

SCMOS Layout Rules - Via2

Vias must be drawn orthogonal to the grid of the layout. Non-Manhattan vias are not allowed.

Rule	Description	Lambda					
		3 Metal Process			4+ Metal Process		
		SCMOS	SUBM	DEEP	SCMOS	SUBM	DEEP
14.1	Exact size	2x2	2x2	n/a	2x2	2x2	3x3
14.2	Minimum spacing	3	3	n/a	3	3	3
14.3	Minimum overlap by metal2	1	1	n/a	1	1	1
14.4	Via2 may be placed over via1						
14.5	Via2 may be placed over contact						
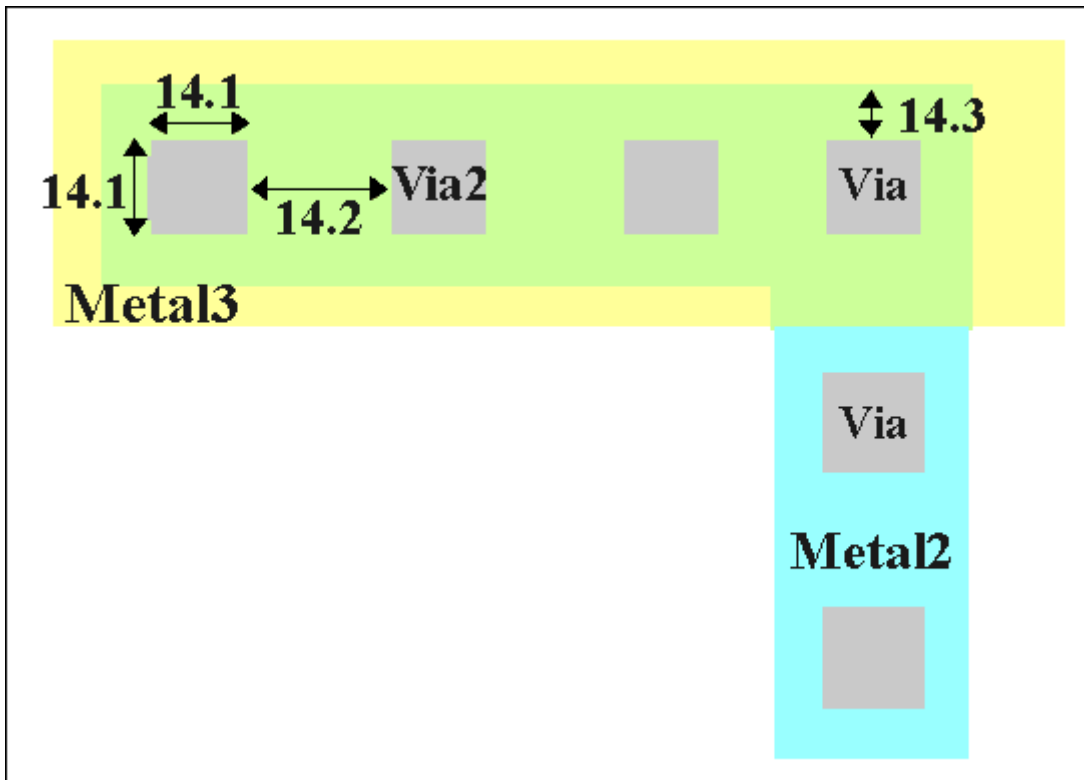
SCMOS Layout Rules - Overglass

Note that rules in this section are in units of microns, **not** lambda. They are not "true" design rules, but they do make good practice rules. Unfortunately, there are no really good generic pad design rules since pads are process-specific.

Rule	Description	Microns (**not** lambda)
10.1	Minimum bonding passivation opening	60
10.2	Minimum probe passivation opening	20
10.3	Pad metal overlap of passivation	6
10.4	Minimum pad spacing to unrelated metal	30
10.5	Minimum pad spacing to active, poly or poly2	15

* "Pad" metal is illustrated as Metal2, but it's really whatever topmost metal layer is available (depends on options).